What is Claimed is:

1. In a target processor, an apparatus for controlling the response to an event, the apparatus comprising:

a central processing unit;

first signal paths from selected apparatus in the central processing unit, the selected apparatus receiving predetermined event signals;

second signal paths from target processor mode identifying the mode of operation a central of the of operation signals

a unit coupled to the first and second signal paths, the unit providing a response to event signals the signals on the second signal paths.

2. The apparatus as recited in claim 1 wherein the unit receives control signals from a user.

3. The apparatus as recited in claim 1 wherein the response to an event signal detected during a first mode of instruction code execution is delayed until a second mode of instruction code execution.

4. The apparatus as recited in claim 3 wherein the first mode of instruction code execution a background mode of instruction execution and a second mode of instruction

execution was a foreground or program mode of instruction execution.

5. The apparatus as recited in claim 1 wherein the unit is a trigger unit and wherein the response to an event signal is the generation of a trigger signal.

6. The apparatus as recited in claim 5 further comprising trace stream generation apparatus, wherein the trigger unit generates a sync signal in response to a trigger signal.

7. The method of responding to an event detected in a target processor, the method comprising:

providing an immediate response to an event detected during a first mode of instruction execution; and

providing a delayed response to an event detected during a second mode of instruction execution, the response to the event delayed until the target processor enters a second mode of instruction execution.

8. The method as recited in claim 7 wherein the first mode of instruction execution is a background or program code execution mode and the second mode of instruction execution is a foreground ground or interrupt service routine program code execution mode.

9. The method as recited in claim 8 further comprising:

in response to first control signals, providing an immediate response to an event during the first and the second mode of code execution.

10. The method as recited in claim 7 wherein the immediate and the delayed response is the generation of a trigger signal.

11. A test and debug system in a target processor, the system comprising:

a central processing unit, the central processing unit generating event signals and mode of operation signals; and

a logic unit responsive to the event signals and to the mode of operation signals, the logic unit providing an immediate response to an event signal in a first mode of operation, the logic unit providing a response to an event signal during second mode of operation in the first mode of operation.

12. The system as recited in claim 11 wherein the first mode of operation is a background or program mode of instruction execution and the second mode of operation is a background or interrupt service routine mode of instruction execution.

13. The system as recited in claim 11 wherein the response is a generation of trigger signal.

14. The system as recited in claim 11 wherein, in response to first control signals, the response of the logic unit to an event is generated immediately in both the first and the second mode of operation.

15. The system as recited in claim 14 further comprising trace stream generating apparatus, the response of the logic unit is the generation of a trigger signal, the trigger signal resulting in a sync marker in the trace stream.